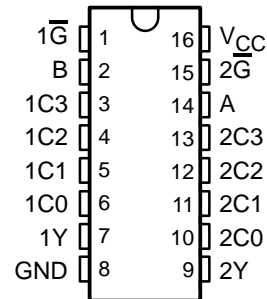


CD54AC153, CD74AC153 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCHS334A – MARCH 2003 - REVISED MAY 2003

- AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ±24-mA Output Drive Current – Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54AC153 . . . F PACKAGE
CD74AC153 . . . E OR M PACKAGE
(TOP VIEW)



description/ordering information

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe (\overline{G}) inputs are provided for each of the two 4-line sections.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74AC153E	CD74AC153E
	SOIC – M	Tube	CD74AC153M	AC153M
		Tape and reel	CD74AC153M96	
	CDIP – F	Tube	CD54AC153F3A	CD54AC153F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS							OUTPUT Y
SELECT‡		DATA				\overline{G}	
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

‡ Select inputs A and B are common to both sections.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

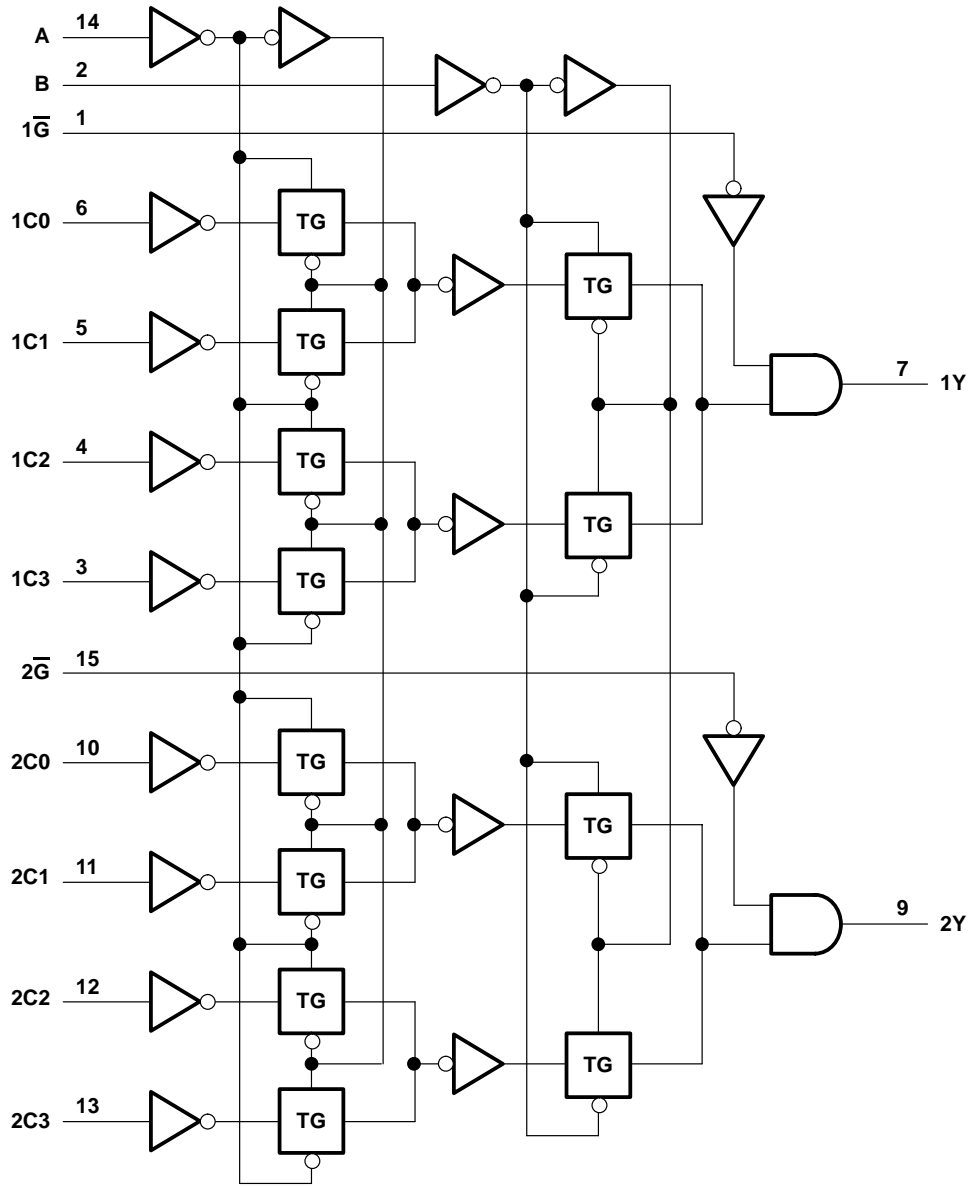
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CD54AC153, CD74AC153 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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logic diagram (positive logic)



CD54AC153, CD74AC153

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	–0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2): E package	67°C/W
M package	73°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		$T_A = 25^\circ\text{C}$		$-55^\circ\text{C to } 125^\circ\text{C}$		$-40^\circ\text{C to } 85^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 1.5\text{ V}$		1.2		1.2		V
		$V_{CC} = 3\text{ V}$		2.1		2.1		
		$V_{CC} = 5.5\text{ V}$		3.85		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 1.5\text{ V}$			0.3		0.3	V
		$V_{CC} = 3\text{ V}$			0.9		0.9	
		$V_{CC} = 5.5\text{ V}$			1.65		1.65	
V_I	Input voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$		–24		–24		mA
I_{OL}	Low-level output current	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$		24		24		mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.5\text{ V to } 3\text{ V}$		50		50		ns/V
		$V_{CC} = 3.6\text{ V to } 5.5\text{ V}$		20		20		

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



CD54AC153, CD74AC153 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -50 μA	1.5 V	1.4	1.4	1.4			V
			3 V	2.9	2.9	2.9			
			4.5 V	4.4	4.4	4.4			
		I _{OH} = -4 mA	3 V	2.58	2.4	2.48			
		I _{OH} = -24 mA	4.5 V	3.94	3.7	3.8			
		I _{OH} = -50 mA†	5.5 V		3.85				
		I _{OH} = -75 mA†	5.5 V			3.85			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 50 μA	1.5 V	0.1	0.1	0.1			V
			3 V	0.1	0.1	0.1			
			4.5 V	0.1	0.1	0.1			
		I _{OL} = 12 mA	3 V	0.36	0.5	0.44			
		I _{OL} = 24 mA	4.5 V	0.36	0.5	0.44			
		I _{OL} = 50 mA†	5.5 V		1.65				
		I _{OL} = 75 mA†	5.5 V			1.65			
I _I	V _I = V _{CC} or GND	5.5 V		±0.1	±1	±1		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		8	160	80		μA	
C _i				10	10	10		pF	

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 1.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	250		227		ns
t _{PHL}			250		227		
t _{PLH}	Any C	Y	166		151		ns
t _{PHL}			166		151		
t _{PLH}	\bar{G}	Y	148		134		ns
t _{PHL}			148		134		



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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	7	28	7.2	25.5	ns
t _{PHL}			7	28	7.2	25.5	
t _{PLH}	Any C	Y	4.7	18.6	4.8	16.9	ns
t _{PHL}			4.7	18.6	4.8	16.9	
t _{PLH}	\bar{G}	Y	4.1	16.5	4.3	15	ns
t _{PHL}			4.1	16.5	4.3	15	

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	5	20	5.2	18.2	ns
t _{PHL}			5	20	5.2	18.2	
t _{PLH}	Any C	Y	3.3	13.3	3.4	12.1	ns
t _{PHL}			3.3	13.3	3.4	12.1	
t _{PLH}	\bar{G}	Y	3	11.8	3.1	10.7	ns
t _{PHL}			3	11.8	3.1	10.7	

operating characteristics, T_A = 25°C

PARAMETER	TYP	UNIT
C _{pd} Power dissipation capacitance	93	pF

CD54AC153, CD74AC153 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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PARAMETER MEASUREMENT INFORMATION



† When $V_{CC} = 1.5\text{ V}$, $R1 = R2 = 1\text{ k}\Omega$

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$. Phase relationships between waveforms are arbitrary.
 - For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD54AC153F3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD74AC153E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74AC153EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74AC153M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC153M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC153M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC153M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC153ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC153MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC153M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC153M96	SOIC	D	16	2500	333.2	345.9	28.6

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

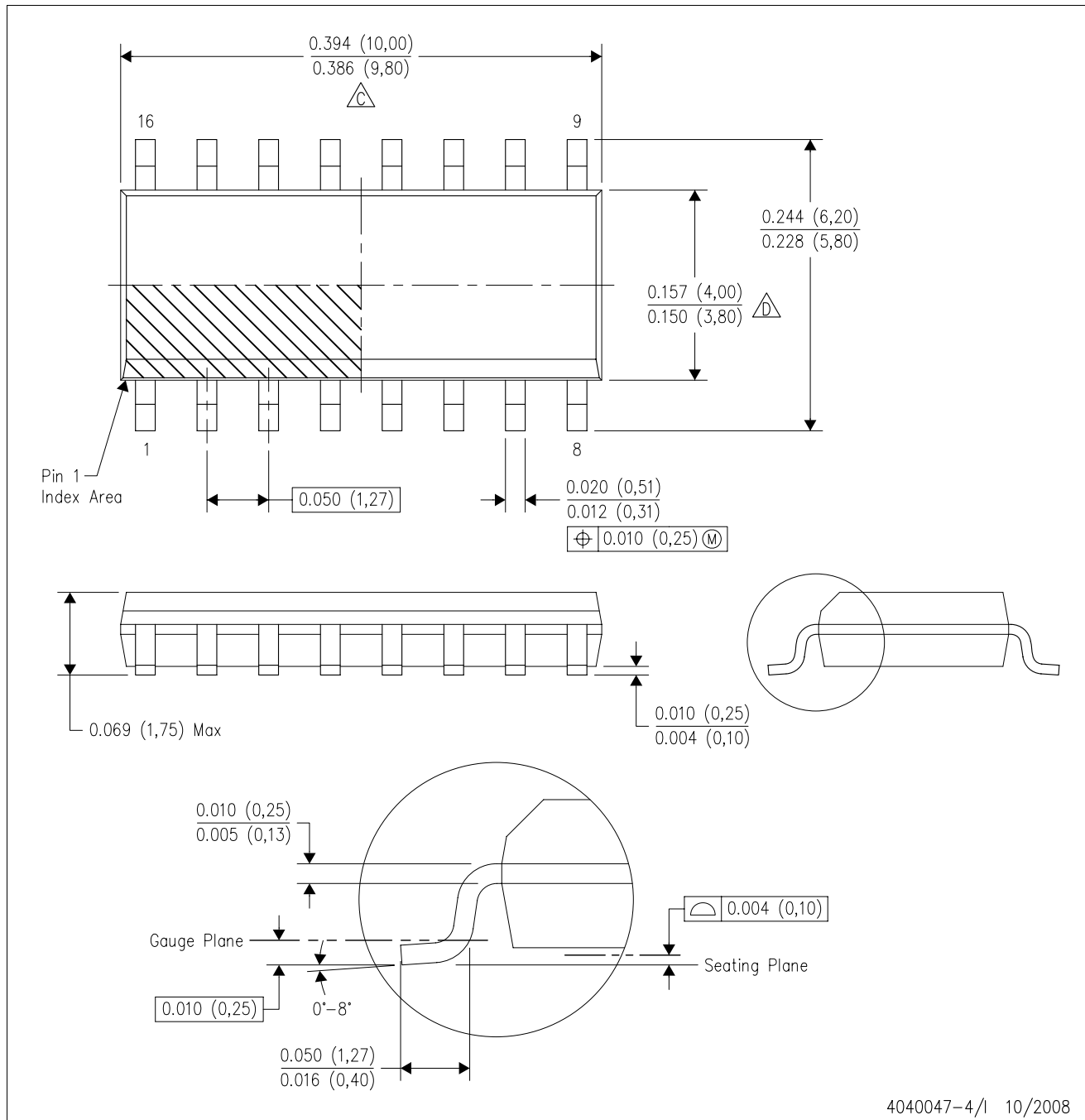


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

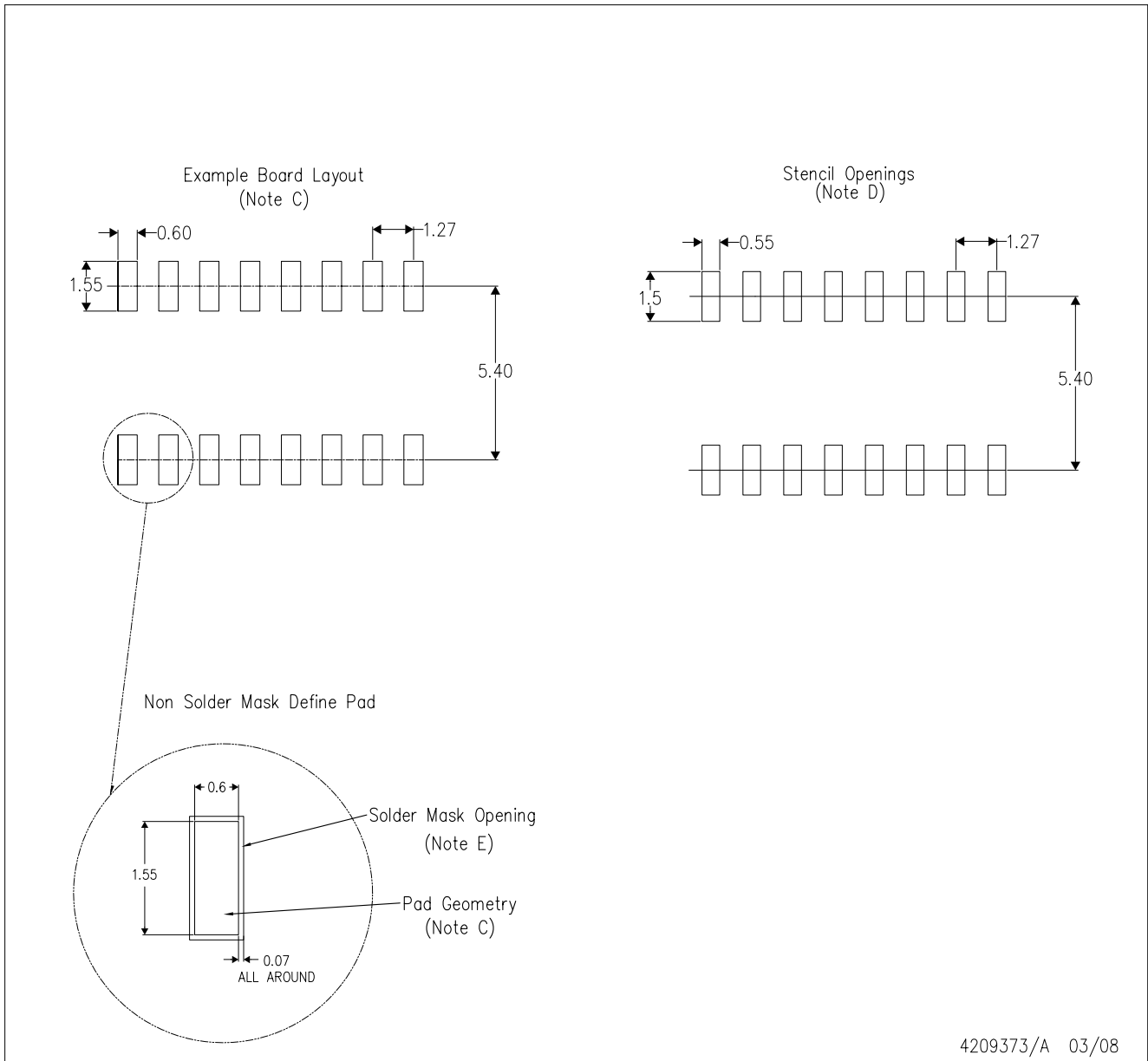
D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



4209373/A 03/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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